

S/N 09/847,479  
Docket: FIS920000077US1

**THE CLAIMS:**

Please amend the claims, as follows:

1. (Currently amended) A method of fabricating an electronic chip on a wafer, comprising:
  - developing on a surface of said wafer a first mask at a predetermined lower resolution;
  - and
  - etching said first mask under a first set of conditions for a predetermined period to achieve a higher resolution mask, said higher resolution achieving a critical dimension that is below 100 nm, said first set of conditions including a tuning parameter to independently control a line width variation tolerance of isolated features relative to nested features,  
wherein said critical dimension is between 75 nm and 100 nm.
2. (Previously presented) The method of claim 1, wherein said first mask comprises an organic photo-sensitive resist material.
3. (Original Claim) The method of claim 1, wherein said first set of conditions comprises an oxygen and nitrogen plasma etch, wherein
  - a flow ratio of oxygen to nitrogen is between 0.25 and 2.5;
  - a setting of an RF power is in the range of 50 to 200 watts; and
  - a setting of a pressure is between 10 and 45 mTorr.
4. (Currently amended) The method of claim 1, further comprising:
  - etching, under a second set of conditions for a second predetermined period, at least one layer of said wafer or at least one layer of material deposited on said wafer under said first

S/N 09/847,479  
Docket: FIS920000077US1

mask, to remove at least a portion of said at least one layer to produce features at said higher resolution.

5. (Original Claim) The method of claim 4, wherein said second set of conditions comprises a CF<sub>4</sub>/ CHF<sub>3</sub>/ Argon based hard-mask process for etching a gate oxide layer.

6. (Original Claim) The method of claim 5, wherein said second set of conditions further comprises a range of 20-80 sccm (standard Cubic Centimeters/Minute) for CF<sub>4</sub>, 5-15 sccm for CHF<sub>3</sub>, and 40-200 sccm for argon.

7. (Currently amended) A method of fabricating at least one electronic device or circuit on a wafer, comprising:

developing a first mask on an outer surface of said wafer or of a layer of material deposited on said surface to define a pattern for at least part of a structure or circuit component for said electronic device or circuit, said first mask comprising an organic photo-sensitive resist material;

performing a trimming process on said first mask to adjust dimensions of said pattern, said trimming process achieving a critical dimension that is less than 100 nm; and

using said trimmed first mask to form a hard mask for an etching process to remove material from at least one layer below said hard mask, wherein

said trimming process includes a tuning parameter to independently control a line width variation tolerance of isolated features relative to nested features,

wherein said critical dimension is between 75 nm and 100 nm.

S/N 09/847,479  
Docket: FIS920000077US1

8. (Original Claim) The method of claim 7, wherein said trimming process of said first mask comprises an oxygen and nitrogen plasma etch, wherein

a flow ratio of oxygen to nitrogen is between 0.25 and 2.5;

a setting of an RF power is in the range of 50 to 200 watts; and

a setting of a pressure is between 10 and 45 mTorr.

9. (Original Claim) The method of claim 7, wherein said etching process to remove material from said at least one layer below said hard mask comprises a CF<sub>4</sub>/ CHF<sub>3</sub>/ Argon based hard-mask process for etching a gate oxide layer.

10. (Original Claim) The method of claim 9, wherein conditions of said etching to remove material off at least one layer below said hard mask comprises a range of 20-80 sccm (standard Cubic Centimeters/Minute) for CF<sub>4</sub>, 5-15 sccm for CHF<sub>3</sub>, and 40-200 sccm for argon.

11. (Currently amended) A method of controlling line width variation tolerances during fabrication of electronic devices or circuits on a wafer, comprising:

developing a first mask on an outer surface of said wafer or of a layer of material deposited on said surface to define a pattern for at least part of a structure or circuit component for said electronic device or circuit, said first mask comprising an organic photo-sensitive resist material;

S/N 09/847,479  
Docket: FIS920000077US1

performing a trimming process on said first mask to adjust dimensions of features of said first mask, said trimming process achieving a critical dimension that is less than 100 nm; and

using said trimmed first mask as a hard mask for an etching process to remove material from at least one layer below said hard mask, wherein

said trimming process of said first mask comprises an oxygen and nitrogen plasma etch, in which:

a flow ratio of oxygen to nitrogen is between 0.25 and 2.5;

a setting of an RF power is in the range of 50 to 200 watts; and

a setting of a pressure is between 10 and 45 mTorr, and

said critical dimension is between 75 nm and 100 nm.

12. (Currently amended) A method, during fabrication of electronic devices or circuits on a wafer, said devices or circuits having both isolated features and nested features, of controlling line width variation tolerances of said isolated features relative to said nested features while independently achieving a target critical dimension that is less than 100 nm, comprising:

establishing a first set of conditions for an RF etch process that achieves said target critical dimension; and

controlling a level of said RF power as a parameter to independently control said line width variation tolerance of said isolated features relative to said nested features,

wherein said first set of conditions comprises an oxygen and nitrogen plasma etch, in which:

a flow ratio of oxygen to nitrogen is between 0.25 and 2.5;

S/N 09/847,479  
Docket: FIS920000077US1

a setting of an RF power is in the range of 50 to 200 watts; and  
a setting of a pressure is between 10 and 45 mTorr, and  
said critical dimension is between 75 nm and 100 nm.

13-20. (Canceled)